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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,569	09/29/2000	Ravi P. Singh	10559/292001/P9299-ADI	3025
20985	7590	01/17/2006	EXAMINER	
FISH & RICHARDSON, PC P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			ROJAS, MIDYS	
			ART UNIT	PAPER NUMBER
			2185	

DATE MAILED: 01/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/675,569	Applicant(s) SINGH ET AL.	
	Examiner Midys Rojas	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7, 9-23 and 27-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13-17 is/are allowed.
- 6) ☒ Claim(s) 1-7, 9-12, 18-23 and 27-34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 August 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>5/25/05 (MR)</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-7, 9-23, and 27-34 have been considered but are moot in view of the new ground(s) of rejection.

Regarding Claim 1, Applicant argues that since Mann's trace compression is done on the basis of disruptions in the program flow, few of Mann's trace entries contain address values and so, one of ordinary skill in the art would not turn to those few trace entries for trace comparison. Additionally, applicant argues that a method of trace comparison for compression would depart from Mann's basis for trace compression. However, since some of Mann's traces do involve address values, a trace comparison compression method could still be used for instances where further compression is desired. Therefore, in the combination of Mann in view of Tanihira and further in view of Bachand, the method of trace comparison compression could be an additional compression method.

In response to applicant's argument that there is no suggestion to combine the references ("suggestion or motivation must be founded in the prior art..."), the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the comparison and blocking operations of Bachand et al. with the system of Mann in view of

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Tanihira because doing so would give the system coherency capabilities and thus allow the trace buffer to avoid storing redundant trace data. Since a trace buffer has limited storage capacity, compression of the captured trace data is desirable [Mann, Col. 18, lines 10-15].

Applicant also argues that Bachand does not disclose comparing a new branch target address in a first holding register to a stored branch target address in a first end register; or comparing a new branch source address in a second holding register to a stored branch source address in a first adjacent register. However, since in Bachand the address of newly requested data from a cell in the snoop queue (first holding register) is compared to the address of a pending-posted transaction from a cell of the transaction queue (first end register); in the following comparison operation, the next address of the newly requested data would come from a second cell in the snoop queue (second holding register) and this would be compared to the address of a second pending-posted transaction from an adjacent cell in the transaction queue (adjacent end register).

Applicant argues that detection logic 246 cannot constitute both a first comparator and a second comparator. Since Bachand uses observation-detection logic, this logic serves the function of a first and second comparator. Detection logic is does not constitute two comparators, but simply performs the function of the two comparators in question.

Applicant also argues that the transaction queue is not a first end register since it is populated by entries of pending bus transactions, not fetches instructions. However, these pending bus transactions are of requests that might have come from the core. In being requested, the data request constitutes a fetch command (request) and therefore, although still pending, they correspond to a fetch command or instruction from the core 100.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-2, 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mann [6,094,729] in view of Tanihira [5,553,010] and further in view of Bachand et al. [US 2003/0115424].

Regarding Claims 1 and 9, Mann discloses a trace buffer 200 [Fig. 2] circuit comprising: a plurality of interconnected registers [Fig. 3], including a first end register to input and output addresses of fetched instructions during a trace operation [the first register of the trace buffer] a second end register [last register of the trace buffer], and a plurality of middle registers connected between said first end and said second end register; Mann does not disclose a write path to shift an instruction address in one of said plurality of interconnected registers by two registers towards the second end register on a write operation.

Tanihira discloses a system in which double shifting is used [Col. 1, line 59-Col. 2, line 10]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the trace buffer of Mann to allow double shifting of data into the buffer in order to ease data input into the buffer [Tanihira Col. 1, lines 27-40]. In the case where this input bus where implemented in the system of Mann, the system would have to push an input from such

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input bus into the trace buffer by two registers [double shifting] in order to accommodate one input of double the size of one register.

Mann in view of Tanihira does not teach first and second holding registers, a first and second comparator, or a compression indication circuit to generate an indicator in response to a new input matching a stored input. Bachand et al. discloses a snoop queue 250 with multiple cells ("first holding register and second holding register"), an external transaction queue 240 with multiple cells ("first end register and first adjacent register"), an observation detection logic ("first/second comparator") to compare the address of the new transaction (from the first holding register in the snoop queue) with addresses of earlier-posted transactions (from the first end register in the transaction queue), and a control logic 254 ("compression indication circuit") to enable the blocking bit, which could be the least significant bit, of the new transaction in response to a match signal (Page 3, paragraphs 0037 - 0038). In this system, a second comparison operation would be performed and so, the next address of the newly requested data would come from a second cell in the snoop queue (second holding register) and this would be compared to the address of a second pending-posted transaction from an adjacent cell in the transaction queue (adjacent end register). Since Bachand uses observation-detection logic, this logic serves the function of a first and second comparator.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the comparison and blocking operations of Bachand et al. with the system of Mann in view of Tanihira because doing so would give the system coherency capabilities and thus allow the trace buffer to avoid storing redundant trace data. Since a trace

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buffer has limited storage capacity, compression of the captured trace data is desirable [Mann, Col. 18, lines 10-15].

Regarding Claim 2, Mann discloses a read path to serial or parallel trace pins 230 in which entries into the trace buffer are shifted one by one [be one register] in a FIFO manner on a read of the trace buffer [Col. 8, lines 1-19].

Regarding Claims 10-11, in the combination of Mann in view of Tanihira in view of Bachand, the trace buffer of Mann would hold the previously posted trace entries. Being that the trace buffer is composed of many registers [Fig. 3] and the observation transaction logic of Bachand is to compare the new transaction with previously posted transactions, the observation transaction logic would act as a comparator for each register of the trace buffer [“third and fourth comparators”]. The control logic 254 [“compression indication circuit”] then enables the blocking bit of the new transaction, which could be a least significant bit, in response to a match signal if a match is detected [Page 3, paragraphs 0037 – 0038].

Regarding Claim 12, the combination of Mann in view of Tanihira in view of Bachand teaches the invention of claim 1 above. Mann discloses a stack comprising a plurality of interconnected flip-flops [Fig. 3], including a first end flip-flop [top of the trace buffer] to input and output valid bits, a second end flip-flop [bottom of the trace buffer], and a plurality of middle flip-flops connected between said first end flip-flop and said second end flip-flop; and a write path coming from core processor 104 to shift a trace in one of said plurality of interconnected flip-flops by one flip-flop pair toward the second end flip-flop on a write operation and a read path coming from serial or parallel trace pins 230 to shift a valid bit by one flip-flop toward the first end flip-flop on a read operation [Col. 8, lines 1-18]. Tanihira discloses

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a system that uses double shifting (see Column 1, line 59 – Column 2, line 10). Although Mann refers to the trace buffer as having registers or entries, flip-flops are a building block of which registers can be made.

4. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mann [6,094,729] in view of Tanihira [5,553,010] in view of Bachand et al. [US 2003/0115424] and further in view of Panagrahi [3,975,717].

Regarding Claim 3, the combination of Mann in view of Tanihira in view of Bachand teaches the invention of claim 1 above. The combination does not teach the trace buffer operating as a FIFO on a write operation and as a LIFO on a read operation. Panagrahi discloses a stack, which operates as a first-first-out [FIFO] register on the write operation and as a last-in-first-out [LIFO] register on the read operation. The system of Panagrahi is capable of both LIFO and FIFO operations and selectively enables read and write operations at either LIFO or FIFO modes [see Abstract]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the trace buffer of the combination of Mann in view of Tanihira in view of Bachand to act as that of Panagrahi thus allowing for the system of place new entries at the top of the buffer [FIFO] while still being able to remove old traces from that end of the buffer [LIFO]. This gives the system more flexibility as to how it can access the captured traces.

Regarding Claims 4-5, the combination of Mann in view of Tanihira in view of Bachand teaches the invention of claim 1 above. The combination does not teach instruction addresses comprising 32-bit words. Panagrahi discloses a stack in which each register pair has the capacity to take in an input the size of a 2^n bit word [Column 3, lines 59-67]. Since “n” can be any

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number, each register and the size of each input [instruction address] can be 32-bits wide. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Mann in view of Tanihira in view of Bachand to include the 32-bit word instructions of Panagrahi since this is a common instruction word size and it allows for faster transmission rates as opposed to smaller word sizes [i.e. 16-bit words]. In this case, “n” would have a value of 16.

Regarding Claim 6, Panagrahi discloses a stack system comprising a plurality of registers 1 through M, where M is not defined. It is understood that M could be 32, thus making the total number of registers 32.

Regarding Claim 7, Panagrahi discloses a stack system with a $2n$ -bit bus to read a $2n$ -bit instruction address from the first end register on the read operation where n can be equal to 16 [Column 4, line 67 – Column 5, line 16]. Panagrahi does not teach a 64-bit write bus to write a 64-bit address pair to the first end register and an adjacent register on the write operation. Tanihira discloses a system that uses double shifting [see Column 1, line 59 – Column 2, line 10]. In the case where the input bus of Tanihira were to be implemented for the trace buffer, the system would have to push an input double the size [64-bit] from such input bus into the stack by shifting the input by two register pairs [double shifting] in order to accommodate one input of double the size of one register pair [32-bit].

5. Claims 18-23 and 27-34 rejected under 35 U.S.C. 103(a) as being unpatentable over Mann [6,094,729] in view of Bachand et al. [US 2003/0115424].

Regarding Claims 18, 20, 27, and 29, Mann discloses performing a trace operation [producing a trace record, see Abstract] including storing fetched instructions in a trace buffer

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200 [see Figures 2 and 3], said storing comprising storing an address pair corresponding to a loop in the trace buffer [Col 15, lines 20-42 “several x86 instructions generate trace records including... LOOP instructions”]. Mann discloses the need for compression operations in trace buffers due to their limited size [Col. 18, lines 10-15]. Mann does not teach a compression operation including a comparison operation. Bachand discloses a snoop queue 250 [“first holding registers”], an external transaction queue 240 [“second holding register”], an observation detection logic [“first/second comparator”] to compare the address of the new transaction in the snoop queue with addresses of earlier-posted transactions in the external transaction queue, and a control logic 254 [“compression indication circuit”] to enable the blocking bit of the new transaction [branch target address] in response to a match signal [Page 3, paragraphs 0033 and 0037 – 0038].

Regarding Claims 19, 23, 28, and 32 Bachand et al. discloses blocking the new transaction [new address pair] in response to the new transaction matching the stored previous transactions. In this case, blocking the transaction is analogous to discarding the transaction since it becomes blocked from usage [“...blocking bit which, if enabled, prevents the snoop queue from issuing a snoop prove” Page 3, paragraph 0033 and 0038].

Regarding Claims 21 and 30, Bachand et al. discloses not blocking the new transaction if it does not match a previous transaction. So, the new transaction will eventually be passed to cache 220 and stored in the internal transaction queue 230 [Page 3, paragraph 0038 – 0041]

Regarding Claims 22 and 31, Bachand et al. discloses comparing the new address pair to the stored address pairs in order to determine if the new address pair matches any of the stored address pairs; since the system check for a match within all the stored address pairs, the new

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address pair must be compared to all the stored address pairs in the system [first, second, third, etc]. Bachand also discloses setting a least significant bit [“blocking bit”] of a branch target address [“new transaction”] in response to the new address pair matching any stored address pair [Page 3, paragraph 0038], and not blocking the new transaction if it does not match a previous transaction. If it is not blocked, the new transaction will eventually be passed to cache 220 and stored in the internal transaction queue 230 [Page 3, paragraph 0038 – 0041].

Regarding Claims 33-34, the new address pair is considered to be a branch target address since it describes the address that the transaction will target, whereas the stored address pair is a branch source address since it describes the address that the earlier posted transaction has already targeted.

Allowable Subject Matter

6. Claims 13-17 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter:

The limitations of independent claim 13 do not appear to be found in the Prior art of Record. The Prior Art does not teach nor suggest in the claimed combination A pipelined processor comprising the limitations of the invention.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

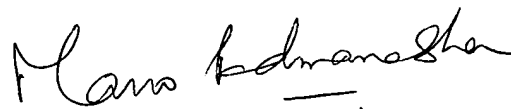
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Midys Rojas
Examiner
Art Unit 2185

MR


1/9/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER